Fermilab FERMILAB-Conf-02/224-E November 2002

Radiation Validation for the CMS HCAL Front-End Electronics

J. Whitmore, A. Baumbaugh, J.E. Elias, S. Holm, K. Knickerbocker, S. Los,
C. Rivetta, A. Ronzhin, A. Shenai, R. Yarema (Presenter), T. Zimmerman

Fermi National Accelerator Laboratory, P.O. Box 500, Batavia, IL, USA
jaws@fnal.gov

Abstract

Over a 10 year operating period, the CMS Hadron Calorimeter (HCAL) detector will be exposed to radiation fields of approximately 1 kRad of total ionizing dose (TID) and a neutron fluence of 4E11 n/cm^2. All front-end electronics must be qualified to survive this radiation environment with no degradation in performance. In addition, digital components in this environment can experience single-event upset (SEU) and single-event latch-up (SEL). A measurement of these single-event effects (SEE) for all components is necessary in order to understand the level that will be encountered. Radiation effects in all electronic components of the HCAL front-end system have been studied. Results from these studies will be presented.

I. The CMS HCAL Radiation Environment

The CMS experiment is scheduled to run for 10 years. During this period, some detector elements will be irradiated with a total ionizing dose (TID) of over 10 MRad and a neutron fluence of over 1E15 n/cm^2. However, the HCAL detector will see a much smaller dose. The highest doses that sections of the HCAL detector will see are ionizing dose of 330 rads and a neutron flux of 1.3E11 n/cm^2 [1]. Since these estimates have uncertainties on th
factor of three and do not include any safety f
dose studies performed probed fluences of 5E11 n/cm^2 and over 1kRad. High energy neutrons that interact in t
are expected to produce an SEE such as SEU or
SEU is defined as a non-destructive event that
flop to change state. An SEL is a potentially
event resulting from triggering a silicon controlled recti
(SCR) formed from the parasitics of the bulk sil

The HCAL detector [2] is a sampling calorimete
absorber and scintillating tile with embedded f
The front-end electronics chain is shown in Figu
photo-diodes (HPD) [3] convert light into cur
presented to a dead timeless integrating ADC
Charge Integrating and Encoding ASIC) [4] runn
MHz. The CCA (Channel Control ASIC) [5] provide
to the QIE and synchronizes and monitors data from mu
QIEs. The GOL (Gigabit Optical Link) performs
to-serial conversion and drives the data to a
Vertical Cavity Surface Emitting Laser (VCSEL).
then optically transmitted out of the radiation a
to the HCAL trigger and readout boards.

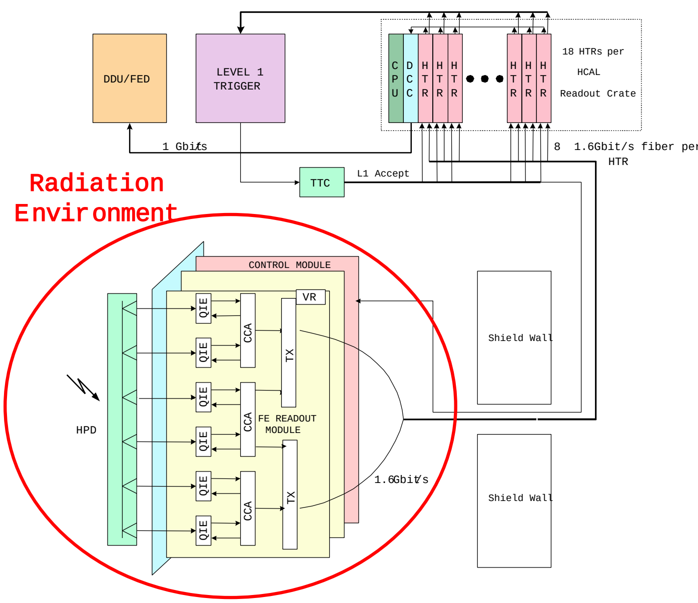

Figure 1: HCAL Front-End Electronics Schematic. TX represents the Gigabit Optical Link and the VCSEL.

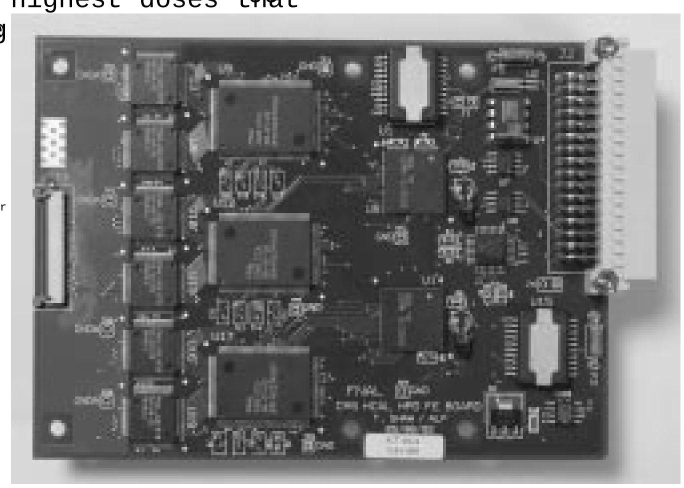

Figure 2: HCAL Six Channel Front-End P.C. Board

A picture of a prototype 6-channel front-en
shown in Figure 2. The major components of the
board are (from left to right): eight QIEs, three CCAs, two GOL
transmitters, two low voltage regulators, and
(mounted on the back side of the board). In additi
front-end boards, Clock Control Monitoring (CCM)
distribute clocks to the front-end boards
temperatures and low voltages, and provide sl
communication paths for downloading control regi

Work supported by the Department of Energy under contract No.DE-AC02-76CH03000.

in the radiation zone are calibration modules that provide monitoring of the front-end electronics path via radioactive source, LED, or laser injection inputs.

The QIE is fabricated in the Austria Micro Systems (AMS) 0.8 µm BiCMOS process. The CCA is fabricated in the Agilent (formerly HP) 0.5 µm micron bulk-CMOS process. The QIE has bipolar and MOS transistors, while the CCA uses only MOS. Bipolar transistors in the AMS process have been studied previously [6], and circuits have been proven tolerant up to 10 MRad ionizing dose. The effects from displacement damage are explored in the studies reported here. SEU susceptibility has been investigated with test shift registers for both the Agilent and AMS processes. Four different flip-flop cell layouts were studied for each process. Results are presented in Section III.

Radiation effects on other major components of this system also have been investigated. Some components, like the GOL and the low voltage regulators, have been developed in radiation hard processes [7,8]. The VCSEL has been tested by the manufacturer to much higher radiation levels than will be seen by HCAL, but with a different packaging; we have studied the VCSEL in the final packaging that will be used in the HCAL system. Single-event Burnout (SEB) was studied for the HPD. Commercial front-end components (FPGAs, PECL clocking chips, transceivers, Analog MUX, temperature sensors, LEDs, VCSELs) were studied for SEE. Components with acceptable SEU levels and limited SEL susceptibility have been selected.

II. Radiation Facility and Procedure

Most of the radiation effects studies reported here were done using the Indiana University Cyclotron Facility (IUCF) 200 MeV proton cyclotron in Bloomington, Indiana. The correlation for bulk damage induced protons at fixed energy and that for the predicted neutron spectrum at the location of the electronics has been calculated [1] for a variety of proton energies. The high-energy proton beam at IUCF was selected as opposed to the more common 60 MeV facilities for several reasons:

- TID is a factor of 2.3 lower per proton allowing higher fluences per test device.
- Linear energy transfers up to 25 MeV-cm^2/mg are reached.
- Ten percent of the interactions have linear energy transfers above 8 MeV-cm^2/mg [9].
- Fission reactions are possible with dopant and impurity species, and can trigger a destructive SEL.

Since typical linear energy transfer figures for the CMS environment are less than 15 MeV-cm^2/mg [10], a device that is insensitive to latch-up in a 200 MeV beam is expected to be immune to latch-up in the CMS environment. Radiation effects studies of low voltage DC-DC converters at 60, 200, and 300 MeV were performed at Louvain-la-Neuve, Belgium, IUCF, and Paul Scherrer Institute, Switzerland, respectively.

Devices under test (DUT) were placed at the beam line and were illuminated with a 7 cm diameter beam spot. Approximately 25 feet away and behind a wall was the test station that provided power t registered the data, reset the devices, and pow DUT if an SEL was sensed. A PC that recorded errors and the number of SEL resets resided in house, approximately 75 feet from the test sta description of the test stand and the IUCF fa found in references [11] and [12].

Irradiations were done in two steps where th took all devices to the full 10-year dose equivalent to as bulk damage issues. Subsequently, the devices irradiated to much higher levels to determine SEU a probabilities with adequate statistics. The SE were assessed using the number of SEE occurre proton times the neutron equivalency factor for energy spectrum. Since SEU and SEL have ma different consequences, that is one spurious dat loss of a significant number of channels, the devices in the customary formula [# SEE/fluenc n/cm^2/10yr) x # devices] is interpreted quite d these two cases. Trigger rates are the main con occurrences but only on a 100 microsecond scale entire front-end electronics system is reset eve of the accelerator and any digital SEU error is SEU, the number of devices is then equal to th channels. By contrast, an SEL event could paralyze a system board and its 144 channels making the number o affected two orders of magnitude higher. Thus testing must take the system boards to much high levels corresponding to this increased vulnerabi considerations intervened during the exposures a activation of the test boards became very high, a measurements reported here set a limit of les radiation induced failure per 4 year interval. note that during the SEL enhanced dosing, device sensitive to the TID effect from using a proton stop operating, but continued irradiation and m latch-up was valid since SEL is a phenomenon o bulk silicon.

III. Agilent and AMS Studies

Shift registers of several different transis configurations were produced in both the Agilent 0.5 µm bulk-CMOS and AMS 0.8 µm BiCMOS processes for these radiation studies. Three to four shift registe were operated simultaneously at 40 MHz while beam was on the device. Data were downloaded at the beginning of run. Data from the register outputs were th through the inputs, clocking through the registe The registers were read out once every 15 secon data pattern was refreshed after every reading. the tally of the number of SEUs per register were logged file after each reading.

The proton beam intensity was selected so statistically significant number of single event observed. The beam was tuned for the Agilent and AMS shift registers individually, slowly increasing the intensity until one to two SEUs were observed per minute of beam incident on the device. The optimal running condition for both processes was determined to be ~6E9 p/cm^2/sec. Most runs lasted ~20 minutes and reached a fluence of 6.4E12 p/cm^2 and a total ionizing dose of 390 kRad.

Devices were tested at nominal operating temperature by surrounding the device with resistors, which were used as heaters. For the HCAL environment, the nominal operating temperature is estimated to be ~45 $^\circ$C.

The three shift registers on the Agilent chip each have a chain of 256 D flip-flops connected in a cascade, three clock drivers, and three output drivers. The first design contains minimum size (0.5µm) devices, the second contains minimum size transistors with a guard ring, and the third the transistors scaled by a factor of two with guard rings added. The Agilent chips operate with a 3.3V power

Data were taken with several Agilent chips under varyi conditions. Runs were taken with the beam nor back of the chip, at an 80° angle with respect to the norm a 45° angle, and at a 180° angle. An alternating pattern and 1s were clocked into the registers for mo separate run was taken in which the data pattern all 1s. The cross section for the device was taking the total number of errors divided by t flip-flops times the fluence. It is effectively getting an upset per flip-flop per n/cm^2. A summary of the run conditions, the fluence, the number of error sections for the Agilent devices is shown in Table 1.

Table 1 Results for Agilent SEU studies. SEU cross-section is calculated by # SEE/fluence (n/c

Dev. No.	Beam Angle	Bit Patt.	TID (kRad)	Fluence (p/cm^2)	Reg. No.	0⇒1	1⇒0	Total Error	X-Sec (cm^2)
1	0	Alt	391	6.44E12	1	42	8	50	0.305E-13
					2	28	3	31	0.189E-13
					3	7	0	7	0.427E-14
3	0	Alt	391	6.44E12	1	43	6	49	0.299E-13
					2	33	8	41	0.250E-13
					3	4	0	4	0.244E-14
5	80	Alt	195	3.2E12	1	25	10	35	0.427E-13
					2	19	1	20	0.244E-13
					3	10	0	10	0.122E-13
5	45	Alt	195	3.2E12	1	30	6	36	0.439E-13
					2	20	1	21	0.256E-13
					3	5	0	5	0.610E-14
2	0	0s	195	3.2E12	1	33	0	33	0.403E-13
					2	19	0	19	0.232E-13
					3	2	0	2	0.244E-14
2	0	1s	195	3.2E12	1	0	4	4	0.488E-14
					2	0	2	2	0.244E-14
					3	0	0	0	<0.122E-14
4	180	Alt	391	6.4E12	1	49	5	54	0.330E-13
					2	28	8	36	0.220E-13
					3	Not a functioning register			

One effect observed was that more upsets occurred in registers with the minimum size transistors than in the register with the larger transistors, when the beam was normal to the chips. There were also fewer upsets for the register that had minimum feature size with guard rings than the one without. As expected, SEU errors of a 0 changing to a 1 occurred more frequently than a 1 changing to a 0. Register 3, which has twice minimum size transistors plus the guard ring, was least sensitive to upsets. However, register 3 was more sensitive to beam angle. This could be the case if the oxide layer were thin, so that there is a large increase in the sensitive volume which a particle passes through when the beam is directed nearly parallel to the face of the chip (as is the case with the 80° run). No latch-ups occurred for any of the registers.

The AMS chip had four shift registers. The first three contained a chain of 256 D flip-flops connected in a cascade. The last register was comprised of 65 D flip-flops connected in a cascade. There were four clock drivers, and four output drivers. The first register had transistors (0.6µm), the second had minimum size plus rings, and the third had transistors scaled by with guard rings. In the fourth case, an SEU to was created. The register contained 65 D flip-flops. The power rail for the AMS chip was 5.0V.

Runs similar to ones taken for the Agilent device were performed. However, the run in which a pattern all 0s was clocked into the device was not carri of the limited number of parts available. Shift 2, i.e. the ones with minimum size transistors, TID during the run. Consequently, the errors, fluence listed in the table for these register delivered at the time that these registers faile SEUs in these two registers were also difficult to determine number of SEUs per reading increased due to the t of shifts in the chip. In order to avoid biasing measurement, a maximum SEU cutoff is set at 5 events reading. This effectively removes the data in which the register is failing from TID. Tests results are summarized in Table 2.

No upsets were ever seen in Register 4, the SEU tolerant register. Register 3, with two times minimum transistor size, is less susceptible to upsets than Registers 1 and 2, which had minimum transistor size. Because registers 1 and 2 failed during the runs in which the beam angle changed to 80° and 45°, it is harder to draw a conclusion about the sensitivity of the smaller transistors to increased beam angle. However, it is apparent that Register 3 is more likely to upset with the beam nearly parallel to the chip. There were no … any of the registers.

A follow-up study was conducted on the AMS c… in order to verify that the failure of the first t… due to ionizing radiation. Chips were tested upo… Fermilab, after ~6 weeks annealing time. Regis… still did not operate. Two of the chips were th… accelerated annealing at 100°C for 154 hrs. This corresp… to ~8 years at room temperature. After ann… registers now work, indicating that the failure … ionizing radiation and not displacement damage.

Table 2. Results for AMS SEU studies.

Dev. No.	Beam Angle	Bit Patt.	TID (kRad)	Fluence (p/cm^2)	Reg. No.	0⟹1	1⟹0	Total Error	X-Sec (cm^2)
4	0	Alt	261	4.30E12	1	64	6	70	0.636E-13
			239	3.94E12	2	43	1	44	0.436E-13
			391	6.44E12	3	2	0	2	0.121E-14
			391	6.44E12	4	0	0	0	<0.243E-14
6	0	Alt	243	4.00E12	1	68	5	73	0.713E-13
			233	3.84E12	2	42	2	44	0.448E-13
			391	6.44E12	3	1	0	1	0.610E-15
			391	6.44E12	4	0	0	0	<0.244E-14
7	80	Alt	194	3.20E12	1	54	14	68	0.830E-13
			184	3.02E12	2	43	3	46	0.595E-13
			194	3.20E12	3	6	0	6	0.732E-14
			194	3.20E12	4	0	0	0	<0.488E-14
7	45	Alt	20	3.20E12	1	11	3	14	0.116E-12
					2	Dead			
			194	3.20E12	3	3	0	3	0.366E-14
			194	3.20E12	4	0	0	0	<0.488E-14
2	180	Alt	218	3.59E12	1	38	4	42	0.457E-13
			203	3.34E12	2	41	5	46	0.538E-13
			391	6.40E12	3	1	0	1	0.610E-15
					4	Not a functioning register			

A test was conducted to measure the effects of displacement damage on bipolar transistors from the AMS 0.8 μm BiCMOS process. The beta of the two NPN transistors on a chip, one minimum size (3μm X 0.8μm) the other larger (29μm X 0.8μm), were measured before irradiation. The transistors were not biased during irradiation. The device was put into the 200 MeV proton beam for a total exposure of 5E11 p/cm^2 corresponding to ~13 kRad ionizing radiation. The betas of the two transistors were re-measured six weeks after exposure. Beta at the operating point of the device, roughly ~10 μA, decreased by 8.6% for the smaller transistor and 11.1% for the larger transistor. Figure 3 shows a plot of beta versus operating current for the minimum size transistor before and after irradiation. The chip was then subjected to accelerated annealing at 100°C and 168 hrs. Beta increased by 2% for the small transistor and 3.4% for the large transistor.

IV. HPD Studies

Studies in which HPDs underwent low energy neutron irradiation to the level that will be seen by the HCAL have been reported on previously [13]. An additional concern was the possibility of single event burnout events (S… that could potentially destroy an HPD. These events could… high energy neutron produces a large energy tra… the HPD silicon near the high field region of … these studies, an HPD was placed in a 200 MeV proton beam and irradiated to the 10 year equivalent exposu… (~2E11 p/cm^2). The HPD bias voltage was varied b… 100V, 150V, and 200V. No dependence on voltage … with no indication of avalanche events. The i… leakage current was consistent with the previ… studies. Details of the SEB study are reported i…

V. Commercial Parts

The Actel A54SX72A FPGA will be used to down… information via the slow data path. For the pu… test, the device was configured as a 256-bit … similar to the AMS-Agilent studies. During irradiatio… devices were monitored for SEU and SEL. FPGAs are … These bipolar parts that are sensitive to TID. Cons… devices stopped functioning after ~150 kRad. The chips were … irradiated further, to set an SEL limit of les… Control Module (CCM) board failure per 4 years o…

SEUs were seen at an acceptable level of 1 SEU per board per week. No SELs were seen, but current draw for a device increased roughly 50-75% after the device stopped functioning. The Philips I2C transceiver (P82B96) was also tested. This part was irradiated to a level that limit to be set of less than 1 SEL per 4 years of operation. The device was also sensitive to TID and stopped working at ~50 kRad, so the SEU data collected were not useful. However, because of the logic levels of the P82B96, we plan to replace the device with the 82B715 Bus Extender. The 82B715 will be tested in October 2002.

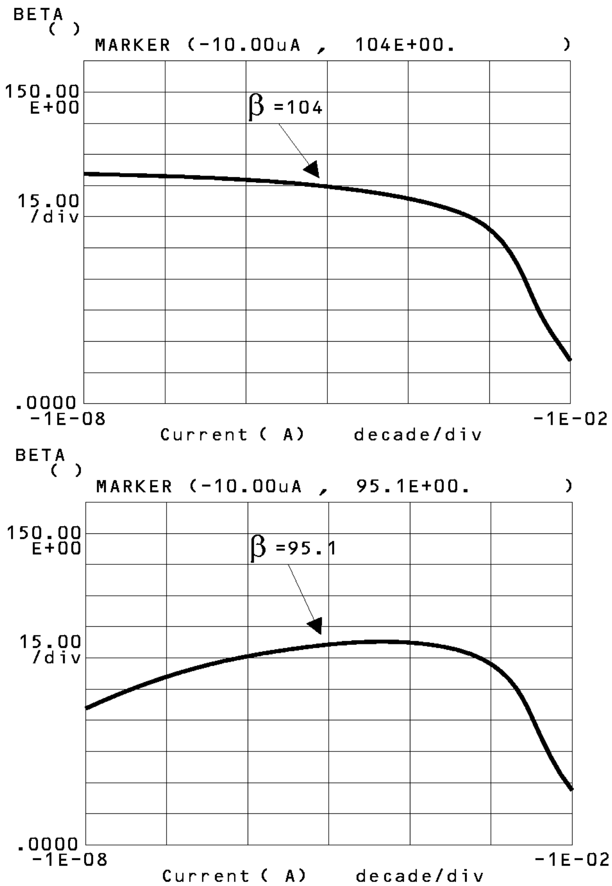

Figure: 3 Beta versus operating current for a minimum size NPN transistor before (top) and after (bottom) irradiation.

An earlier study of clocking devices showed BLVDS chips (National MCDS92LV090A and DS92CK16) were sensitive to SEL. PECL chips, however, were insensitive to irradiation and have been selected for the HCAL front-end boards. All devices were operated at 40 MHz during irradiation. Clock glitches were monitored with a high-speed scope. Latch-up was monitored with automatic power cycling of the chip if over-current was sensed. Several different Motorola clock chips were studied: MC100LVEP111 (differential PECL clock driver), MC100LVELT23 (dual differential LVPECL-LVTTL), and the MC100LVELT22 (dual differential LVTTL-LVPECL). Chips were irradiated to a level that set limits of less than 1 failure per 4 year operating period for either a 6-channel board or a CCM module.

Low voltage Vicor DC-DC converters (V375B5C200A, V375B12C250A, V300B12C250AL, V300B5C200A) were studied for radiation tolerance against destruct irradiated up to 2E11 p/cm² with protons of 60 MeV, 200MeV, and 300MeV protons. SEB induced failures seem to for V375B5C200A and V300B12C250AL, although converters appeared to perform well up to fluences of 1.0-3.0E11 p/cm² if the input voltage, V_{as}, were in the range c 255-300V. All converters operated without fai minimal neutron fluence when de-rating the input output voltages. Results are presented in [15].

Honeywell HFE419x-521 VCSELs have been selected fo the HCAL readout system. Honeywell VCSELs with the same glass have been irradiated to more than 100 MRads with less than 14% degradation for chip and glass combined pack version of the HFE419x-521 also has been i more than 10 MRads with no darkening observed [16]. studies, several VCSELs were exposed to 200 MeV protons at IUCF with 5E11 p/cm2 (~8 kRad). Data transmission integrity after dosing was tested at 1.6 Gbps operation. No bit errors were observed, lending additional confide devices will be robust in the HCAL radiation env

Other support components such as the Analog ADG706 analog MUX were tested. No latch-ups we A limit of less than 1 failure per CCM for a 4 year operating perio was achieved. SEUs were observed, but since this dev be used in slow control, the rate was determine tolerable level. Two different types of LEDs were studied. A blue Toshiba (25-365C) and a green Nichia (NS LED were irradiated to the 10 year dose equivalent. S these calibration LEDs will be monitored with PIN-dio the critical factor is that a large drop in lig occur. No significant change in light level was

VI. SUMMARY

Nearly all HCAL front-end electronics compone been radiation proven to operate up to the HCA levels of 4E11 n/cm² and 1 kRad. Additional studies destructive events such as SEL have shown th devices are immune to SEL during a 4 year operating perioc A more stringent specification requiring no SEL of operation was difficult to achieve because of time and the resulting activation of the test registers developed in the Agilent and AMS processes th will be used for the QIE and CCA ASICs were exp 200MeV proton beam. AMS NPN bipolar transistor dosed to 5E11 n/cm² equivalent; a 5-10% drop in the the transistors was seen with no degradation in For a conservative design of twice the minimum and guard ring, SEU cross-sections of 1E-15 SEU per n/cm² per cell were measured, corresponding to ar of 0.1-0.01 SEU/chip/year for a complex layout o An SEU tolerant cell design [17] was implement expected to yield an even lower SEU rate. commercial devices, limits have been set of les per 6-channel (or CCM) board per 4 years. Vicor DC-DC converters can be made radiation tolerant to environment by de-rating the input and output voltages. No indication of avalanche effects in HPDs was seen. Commercial support components for the front-end board have been irradiated and radiation tolerant devices have been selected. Irradiation studies on production layout front-end boards will be conducted in late autumn 2002.

VII. ACKNOWLEDGEMENTS

We would like to thank the staff at Indiana University Cyclotron for the use of their facilities. In particular, we would like to thank Chuck Foster and Ken Nelson of IUCF for their help in conducting these studies.

VIII. REFERENCES

[1] F. Faccio, et al., "A Global Radiation Test Plan for CMS Electronics in HCAL, Muons and Experimental Hall," http://cmsdoc.cern.ch/~faccio/presprop.pdf

M. Huhtinen, "Radiation Environment in Experimental (CMS) Area," Radiation Effects Course, http://rd49.web.cern.ch/RD49/MaterialRadCourse/MHuhtinen2.pdf, 10 April, 2000.

[2] CMS, The Hadron Calorimeter Technical Design Report, CERN/LHCC 97-31, June 20, 1997.

[3] P. Cushman, et al., Nucl. Instrum. Meth. A442: 289-294, 2000.

[4] A. Baumbaugh, Proc. of 4th Workshop on Electronics for LHC Experiments (LEB98), Rome, 21-25 Sep 1998.

[5] R. Yarema, et al., these proceedings.

[6] D. J. White, et al., Nucl. Instrum. Meth. A457:369:377, 2001.

[7] P. Moreira, et al., Proc. of 7th Workshop on Electronics for LHC Experiments, Stockholm, Sweden, 10-14 Sep 2001.

[8] G. Donna, et al., Proc. of 5th Workshop on Electro for the LHC Experiments (LEB 99), Snowmass, Colorado, 20-24 Sep 1999.

[9] P. M. O'Neill, et al., IEEE Trans. Nucl. Sci., vol. 44, pp. 2311-2314, Dec. 1997.

G. D. Badhwar and P.M. O'Neill, Nucl. Instrum. Meth. Phys Res. A 466(3) 464-474, 2001.

[10] J. Kinnison, "COTS in CMS Workshop," present at the CMS Cots Workshop, http://cmsdoc.cern.ch/~gst/cmscots/JKinnison_sli

[11] A. Baumbaugh, Nucl. Instrum. Meth. A409: 275-277, 1998.

[12] C. Foster, et al., Proc. of 14th International Conference on the Application of Accelerators in and Industry, April, 1997.

[13] P. Cushman, et al., Nucl. Instrum. Meth. A411: 304-313, 1998.

[14] A. Baumbaugh, et al., "Results of Hybrid Irradiation by 200-MeV Protons," FERMILAB-TM-216 Dec 2001.

[15] C. Rivetta et al., "Single Event Burnout in DC-DC Converters for the LHC Experiments," FERMILAB-CON 01-250-E, Sep 2001. Presented at RADECS 2001, Grenoble, France, Sep 10-14, 2001.

[16] R. Khurana, Honeywell Engineer, private communication.

[17] M. N. Liu, et al., IEEE Trans. Nucl. Sci. 39, No. 6, p. 1679